Remarks/Arguments

Applicant thanks Examiner Mandala again for his careful examination and clear explanation of the claim rejections. In response, applicant amends claims 29, 33, and 35 to distinguish over the references cited in the Office action. Applicant also cancels claims 34 and 36. Detailed explanation of the amendments follows:

1. Claim 29 stands rejected under 35 U.S.C. 102(b) as being anticipated by the Matsumoto reference and the Nakajima reference; it further stands rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Bertrand reference.

   As amended, claim 29 describes a semiconductor device that has an NMOS transistor gate structure and a PMOS transistor gate structure.

   The NMOS transistor gate structure has a gate dielectric above a semiconductor body, an n-doped first metal silicide structure having a first composition contacting the gate dielectric, and a second metal silicide having a different composition above the n-doped first metal silicide; the PMOS transistor gate structure also has a gate dielectric above a semiconductor body, a p-doped first metal silicide structure having a second composition contacting the gate dielectric, and a second metal silicide having a different composition above the p-doped first metal silicide.

   The Matsumoto reference discloses a semiconductor device in which mutual diffusion of doped impurities through an upper silicide electrode layer is prevented. The device in the Matsumoto reference has one metal silicide layer. It does not have a first metal silicide structure having a first composition and a second metal silicide having a different composition above the first metal silicide. Also, the metal silicide in the Matsumoto device does not contact the gate dielectric. Because the Matsumoto reference fails to disclose at least these limitations, it does not anticipate claim 29.

   The Nakajima reference discloses a method of forming a conductive layer over a gate dielectric. The passages cited in the Office action are copied below:

   > A semiconductor device of the present invention has conductive thin films and is characterized by the following. (1) At least a part of the thin-film has a laminated structure divided along a film thickness direction, and each of the divided layers has

a main component made of the same element or the same compound. (It is desirable that the main component is a material including silicon atom or metal silicide. The material of each layer may be different from that of the other by doping). (2) At least a part of the thin-film has a laminated structure divided along a film thickness direction, and an average crystal grain size of the grains within each one of the divided layers is about 1/2 times to about ten times of the thickness of the divided layer. (For example, the grain size is equal to the thickness of the divided film or is in the same order or is about a fraction or several times as the divided film thickness.) (3) Additionally, or alternately, at least a part of the thin-film has a laminated structure divided along a film thickness direction, and the thickness of each layer is not larger than a thickness prescribed by a critical stress value that is determined according to a fail event of the semiconductor device.[1]

* * *

The method of manufacturing the semiconductor device 1 will be explained by taking an example of manufacturing a CMOS on the p-type silicon semiconductor substrate 4 by referring to cross sectional views of the manufacturing process shown in FIGS. 2 to 14.

A first process is shown in FIG. 2. The surface of the p-type silicon semiconductor substrate 4 is thermally oxidized to form a silicon oxide film 5a. Next, a silicon nitride film 11a is deposited on the surface of the silicon oxide film 5a by a CVD (chemical vapor deposition) or the like.[2]

* * *

FIG. 27 shows a photograph, of an example of an observation by an electron microscope of thin film having a structure of divided polycrystalline layers laminated which has been formed by depositing amorphous silicon and crystalline cobalt layers alternately and then forming polycrystalline layers with columnar by a primary recrystallization reaction. Its magnification is about 180 thousand times.[3]

* * *

A method of manufacturing a thin film according to the present invention will be explained with reference to FIGS. 26, 27, 28 and 29. FIG. 26 explains a flow of the manufacturing of metal silicide thin film according to the present embodiment. In the present method of manufacturing a thin film, a metal silicide thin film of a composition MSi_x (where M is a metal element) is obtained by a chemical reaction of

$$M+xSi=MSi_x.$$

[1] US 5,444,302, col. 3, ll. 20-40.
[2] Id., col. 11, ll. 3-13.
[3] Id., col. 13, ll. 4-11.

After forming a ground film (a silicon oxide film) 5 on a substrate 4, a silicon thin film 6 of a film thickness 1/2 tSi is deposited. In this case, the film thickness tSi is determined by determining a ratio (1:y) of film thickness between a metal thin film 20 and the silicon thin film 6 from a density ratio of each element so that the ratio of atoms becomes

M:Si=1:x

when the composition of the metal silicide film to be finally obtained is MSi.sub.x (where M is a metal element). In other words, the following relation is obtained:

tM:tSi=1:y (1)

Consider a ratio (1:z) of a film thickness tMSi which is two times the film thickness calculated from the thickness of the metal silicide thin film per one layer to be prescribed by a fail event to be obtained in the end to a film thickness of the sum of the film thickness tSi of the silicon thin film and the film thickness tM of the metal thin film, that is

tMSi: (tSi+tM)=1:z (2)

By eliminating tM from the expressions (1) and (2), the following expression is obtained:

tSi=(yz)tMSi/(1+y) (3)

Then a metal thin film to be determined by a film thickness shown below is deposited as the film of the second layer

tM=ztMSi/(1+y) (4)

For a third layer, a silicon thin film of the film thickness tSi is deposited. The metal thin film 20 of the film thickness tM and the silicon thin film 6 of the film thickness tSi are deposited alternately by a necessary number of layers (N layers). The number of layers (considering a pair of the metal thin film and the silicon thin film as one layer) necessary for depositing becomes an integer which satisfies

N=TM/tMSi

when the film thickness of the metal silicide thin film to be obtained in the end is tM. However, tMSi is adjusted so that N becomes an integer at a film thickness not higher than the critical film thickness to be prescribed by a fail event.

The film thickness of the top layer is set to be 1/2 tSi or 1/2 tM. The reason for the film thickness of the bottom layer and the top layer becoming 1/2 is as follows. Since a chemical reaction starts from the interface of different kinds of materials,

the chemical reaction progresses from both sides of the upper interface and the lower interface for both the silicon thin film 6 and the metal thin film 20.

Accordingly, about the half film thickness of each film is consumed by a reaction from the upper interface and the lower interface. In other words, only one side of a reaction interface exists in the top layer film or the bottom layer film so that the necessary film thickness becomes 1/2.

Although the material of the top layer is a silicon thin film which is the same as the bottom layer according to the present embodiment, this need not be a silicon thin film but a metal thin film may also be good. Further, the film of the bottom layer need not be a silicon thin film but the depositing may be started from a metal thin film. Further, the method of depositing each film is not particularly limited.

After completing the depositing by a predetermined number of layers, the whole substrate is heated to a temperature sufficient enough to progress the silicide reaction and then the silicide reaction is completed. An example of the observation of the crystal state of the film after completing the reaction is shown in FIG. 27. FIG. 27 is an example of the observation, by using a transmission electron microscope, of the crystal structure of a film of laminated layers after a thermal annealing of the film at a temperature not lower than the temperature at which a silicide reaction is completed (for example 700.degree. C.) by using a cobalt (Co) thin film as the metal thin film and setting the ratio of the atomic weight as Co: Si=2: 1. A layer i shows a bonding agent for a sample of the transmission electron microscope, a layer ii shows a cobalt silicon alloy laminated film (Co.sub.2 Si) made of about 10 layers in the picture of FIG. 27, a layer iii shows a silicon oxide film and a layer iv shows a silicon substrate. The layer ii shows a state of divided lamination but this is only a color tone difference for each crystal because of difference in crystal orientation.

In a state after the completion of the reaction, it is clear that films have been formed in a laminated structure in a thickness direction of which layer crystal grains linked in horizontal direction pierce in a film thickness direction. The thickness of each film corresponds to a silicide film thickness which is determined by 1/2 of the sum of the film thickness of the metal thin films and silicon thin films that were laminated before the reaction, that is:

$$tMSi=1/2\ (tM+tSi)$$

As described above, when a silicide reaction is carried out after laminating metal thin films and silicon thin films in a plurality of divided lamination, it is possible to obtain a silicide thin film of a predetermined film thickness in a small crystal grain size, that is, in a low stress state in which a fail event does not occur, or stress due to a change in volume during progressing of a silicide reaction.

FIG. 28 shows a cross section of a MOS (metal-oxide-semiconductor) transistor manufactured by applying the present manufacturing method, which shows a state

that a silicide alloy has been used for a gate electrode of the transistor.

> According to the present embodiment, a gate electrode of a predetermined film thickness is formed by a laminated film made of small crystal grains so that the stress at the time of manufacturing a silicide film can be controlled to be not higher than the stress at the time of an occurrence of a fail event.[4]

In summary, the Nakajima reference discloses a method of forming a cobalt silicide film in a semiconductor device with a reduced stress in the film. The reference does not, however, discloses a semiconductor device that has an NMOS transistor gate structure and a PMOS transistor gate structure of specific structure and composition. Therefore, Nakajima reference can not anticipate claim 29 as amended.

Regarding the 103(a) obviousness rejection, applicant respectfully submits that claim 29, as amended, overcomes the rejection. Both the Matsumoto reference and the Bertrand reference do not disclose a gate structure that has a conductivity-specifically doped metal silicide gate electrode contacting the gate dielectric.

Because claim 29, as amended, overcomes the anticipation rejection and the obviousness rejection, it stands patentable over the references.

2. Claims 30-33 all depend directly or indirectly on patentable claim 29. They stand patentable at least by virtue of their dependency. In addition, claim 33 further comprises silicon between the first metal silicide and the second metal silicide. This limitation is not disclosed in any of the references.

3. Claim 35 stands rejected under 35 U.S.C. 102(b) as being anticipated by the Matsumoto reference and the Nakajima reference. Applicant respectfully submits that, as amended, claim 35 overcomes the rejections.

Claim 35 describes a transistor gate structure that includes a gate dielectric, a first metal silicide, and a second metal silicide. The first metal silicide contacts the gate dielectric; is doped with substantially single polarity impurities. The second metal

[4] Id., col. 17, l.50 – col. 19, l. 51.

silicide of the gate structure has a composition different from that of the first metal silicide.

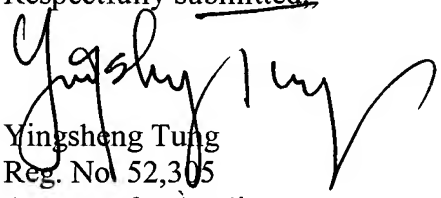
The Matsumoto reference fails to disclose the two-layered silicide structure. It also fails to disclose the first metal silicide being in contact with the gate dielectric. The Nakajima reference fails to disclose the doping limitation of the first metal silicide and it fails to disclose the composition of the two silicide layers being different.

Because both references fail to disclose all the limitations of claim 35, they do not anticipate claim 35.

4. Claims 37-41 depend directly or indirectly on patentable claim 35. By virtue of their dependency, they also stand patentable. Furthermore, claims 37-41 comprise additional limitations. In particular, claim 37 further comprises silicon between the silicide layers, and claims 38-41 further limit the composition of the silicide layers.

In conclusion, applicant respectfully submits that the application is in allowable form and all pending claims distinguish over the cited references. Applicants respectfully request further examination of this application and timely allowance of the pending claims.

Respectfully submitted,



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